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Impact of emitter fabrication on the yield of SiGe HBTs

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ABSTRACT

Epitaxially-grown, *in-situ* doped emitters used for SiGe HBT fabrication deliver a couple of advantages regarding device performance. Positive effects on emitter resistance, low-frequency noise, emitter-collector breakdown and manufacturability are observed. Here we report, that the removing of the interfacial oxide between the capping Si layer of the base and the emitter layer may have significant impact not only on the As indiffusion but also on the yield of small transistors. Depending on the device geometry, the high-temperature treatment of the heavily As doped emitter layers has proven as critical process step regarding the defect formation.

1. Introduction

SiGe HBTs have been found widespread in high-speed wired communications and microwave wireless applications. Low-parasitic device constructions combined with aggressively-scaled vertical doping profiles for the base and the collector led to substantially improved high-frequency capabilities. In addition, modifications of the emitter fabrication boosted the HBT RF performance.

Traditionally, an implanted or *in-situ* doped poly-Si layer was used to form the emitter electrode. The properties of the poly-Si emitter are influenced essentially by an interfacial oxide layer between the polycrystalline part of the emitter and the monocrystalline part formed by the indiffused emitter dopants. Recently, epitaxially-grown emitter layers were realized for SiGe HBTs [1–5]. Primary reasons for the introduction of a mono-Si emitter are the following effects: A lower emitter resistance R_E, reduced low-frequency (LF) noise ($1/f$ noise), higher base currents (leading to higher BV_{CEo}), a lower temperature dependence of the current gain β, and an improved manufacturability.

The fabrication of epitaxial emitters can be achieved by pre-epi cleaning with HF last or *in-situ* cleaning possibly in combination with H_2 pre-bakes. Epitaxial growth does not need perfectly oxygen-free surfaces. In this paper we will show that certain doses of residual oxide have no or minor impact on R_E, LF noise or the base-current level. In contrast, it can have significant impact not only on indiffusion of emitter dopants but also on the yield of small transistors.

2. Device fabrication

For this study we are using IHP's 0.25 µm BiCMOS technology SG25H1. More details of the process are described elsewhere [6]. Here, our focus is directed to the emitter fabrication. Before the emitter process starts, a Si buffer layer, the SiGe:C base layer, and a Si cap layer are deposited. Please note, that the Ge profile consists of a plateau region on the collector side and a graded part towards the emitter. The emitter window is patterned on an oxide/poly-Si layer stack opened by a combination of dry and wet etching (Fig. 1a). A RCA/HF-last cleaning prepares the deposition of an *in-situ* As doped emitter layer. In this paper, we present results for HBTs varying in the emitter fabrication. We compare emitter depositions on a vertical furnace batch tool and on an ASM Epsilon CVD reactor with single wafer processing, respectively. The As concentrations amount to about 3×10^{20} cm^{-3} for the batch tool, and 1×10^{20} cm^{-3} for the single wafer equipment. For both tools, the emitter layers are characterized by monocrystalline grown regions adjacent to the Si cap and polycrystalline parts on top of the poly-Si auxiliary layer (Fig. 2). For depositions on the batch tool, an interfacial oxygen dose of about 5×10^{14} cm^{-2} was measured by SIMS. We determined ~1×10^{14} cm^{-2} for samples fabricated without bake in the single wafer tool. A different kind of emitter, showing no oxygen at the interface, is achieved by applying an additional H_2 pre-bake at 800 °C.

The emitter-base formation is continued by patterning a resist mask to structure the emitter layer and to implant the extrinsic base

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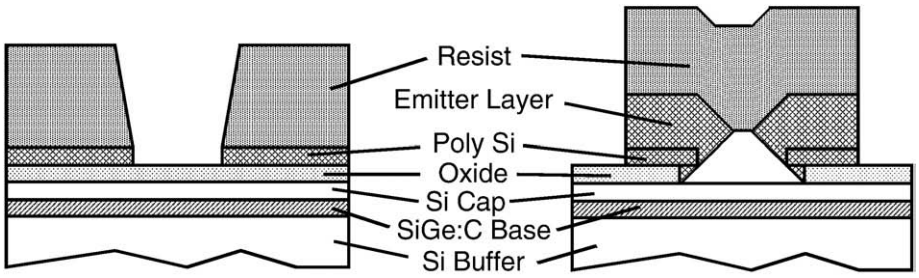

Fig. 1. Schematic cross-sections of the emitter process flow. a) Emitter window opening and b) emitter polystructuring.

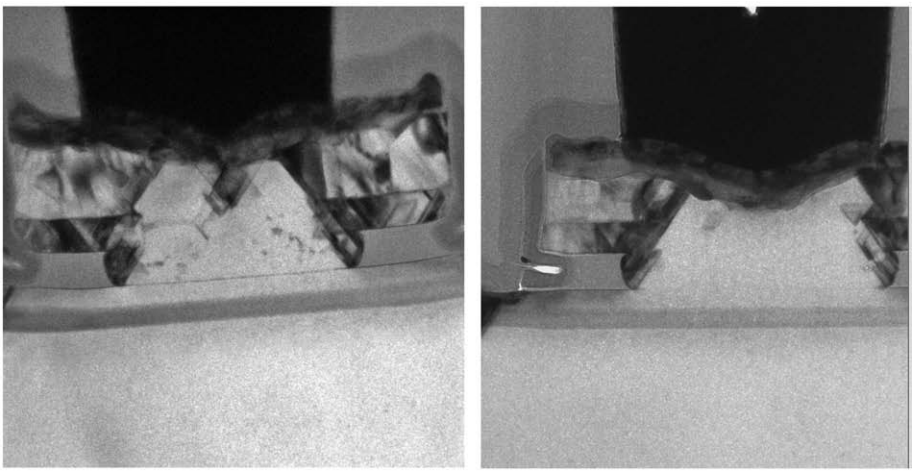

Fig. 2. TEM cross-sections of a) the emitter deposited on the batch tool and b) on the single wafer tool without pre-bake.

(Fig. 1b). The crucial thermal treatment of the emitter represents the final RTP step of about 1000 °C that activates the MOS gate/source/drain regions and controls the indiffusion of the emitter dopants.

3. Device results

First, we evaluate the three emitter deposition splits (batch tool, single wafer tool with and without pre-bake) in terms of emitter resistance R_E, base-current level, indiffusion of emitter dopants and low-frequency (LF) noise. Finally, we will describe the impact of emitter fabrication on the HBT yield.

At least for R_E, LF noise and base-current level one could expect marked differences depending on the interfacial oxygen level. However, we found very similar values of $R_E \sim (23 \pm 1)\Omega$ ($A_{E,\,drawn} = 0.18 \times 0.84\ \mu m^2$) for the different emitter processes. Also the power spectral density of the base-current S_{IB} does not show significant discrepancies (Fig. 3).

Fig. 4 shows Gummel plots of large area transistors. While the base-current level at $V_{BE} = 0.6$ V is almost identical, base-current ideality improves with decreasing interfacial oxide. This effect is only indirectly caused by residual oxide. As we learned from CV measurements, the lower the oxide dose at the interface the lower the As indiffusion into the base cap layer. Taking into account that the base-emitter depletion width for the cases with residual interfacial oxide is smaller than 20 nm, we attribute the nonideality of I_B to tunneling effects [7]. Moreover, we observed a decrease of the collector current I_C by ~30% for small and large transistors when the pre-bake was applied. This is attributed to an enhanced diffusion of boron into regions of lower Ge concentration compared to the cases without pre-bake or the batch tool emitter.

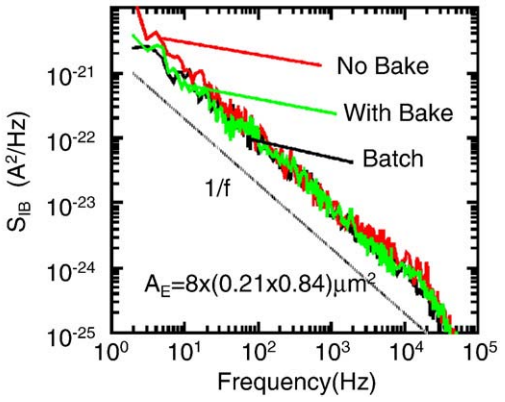

Fig. 3. Power spectral density of base-current noise vs. frequency for different emitter depositions at $I_B = 1$ µA.

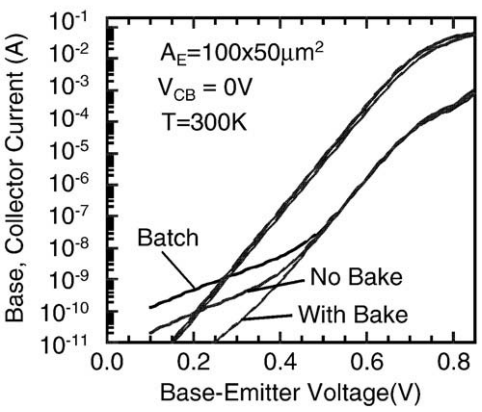

Fig. 4. Gummel plots of large area devices for different emitter depositions at $V_{CB} = 0$ V.

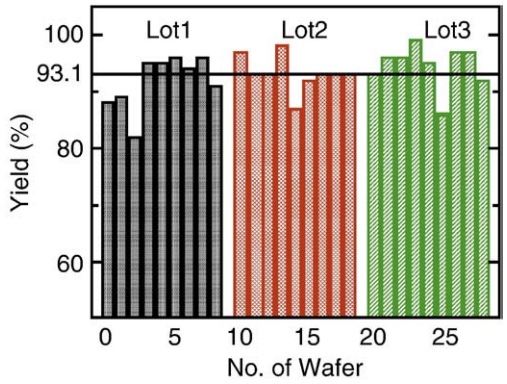

Fig. 5. Yield data of 4k HBT arrays for three lots (in total 2700 arrays) fabricated in SG25H1. One array: A_E=4096×(0.21×0.84) μm^2. Yield criterion: I_{CEs}<1 μA at V_{CB}=2 V.

Fig. 5 shows a yield chart of 4k HBT arrays for three lots fabricated in the SG25H1 process using the batch tool for the emitter deposition. On average 93.1% of 100 arrays per wafer passed the yield criterion of I_{Ces}<1 μA at V_{CB}=2 V. In contrast to the batch tool emitter, we obtained only 60 to 80% yield for the single wafer tool devices without pre-bake, and only 10–20% with bake. The Gummel plots of the defective devices indicate a pipe-like behavior, that means an emitter-collector shortening (Fig. 6). Contrary to the 4k arrays, the way of the emitter fabrication does not cause yield differences for large transistors although these devices surpass with 100×50 μm^2 the total emitter area of the 4k array by a factor of 4. In order to enlighten the circumstances responsible for the defect generation we performed several experiments that are described below.

First, we studied the role of the pre-bake. Split wafers were treated in the single wafer tool only with the bake sequence before the emitter layer was deposited in the batch tool leaving the known amount of oxide at the interface. In this case neither remarkable yield degradation nor device parameter shift was found. Consequently, the thermal budget of the bake does not cause the I_C reduction mentioned before. Second, we skipped the final RTA step for split wafers with pre-bake and emitter deposition in the single wafer tool. For a third split we substituted the *in-situ* As doping by phosphorous. In both cases, an array yield of nearly 100% was achieved. The number of defective devices decreased also considerably when the As concentration was reduced to below 5×10^{19} cm^{-3}. We conclude that the behavior of a highly-concentrated As layer during the final RTA causes an enhanced defect sensitivity of the small area transistors. In this case, local strain effects can generate crystal defects. Obviously, a higher amount of oxygen at the interface can help to prevent defect generation. The microscopic process of the described defect generation and of the reduction of collector currents is not fully understood yet. We assume that the generation of crystal defects and the enhanced boron diffusion are triggered by point defects emitted from the heavily arsenic-doped layer during thermal treatments following the emitter deposition. A certain fraction of the interstitially incorporated As will be activated during the high-temperature RTA step. Moreover, partial deactivation of As during medium-temperature steps in the back-end-of-line process is known to generate Si self-interstitials. However, it is not clear to what extent these processes can lead in combination with an existing local strain field to the formation of dislocations through the SiGe base.

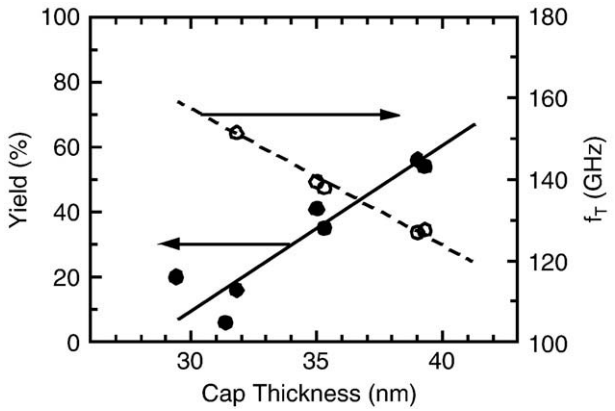

Fig. 7. Yield data of 12k HBT arrays (filled symbols) and peak f_T of single devices (open symbols) vs. base cap thickness related to the standard value. Emitter area of the array: A_E=12,800×(0.18×0.84) μm^2. Yield criterion: ideality of collector current nI_C (at V_{BE}=0.5 V)<1.1.

It remains the question under which conditions it is possible to introduce a highly-doped As emitter with oxygen-free interface without detrimental effects? We observed that the array yield can be increased by increasing the thickness of the base cap layer as shown in Fig. 7. Here, we used the ideality factor of the collector current nI_C at V_{BE}=0.5 V for evaluating the yield. This value is more suitable than the standard specification of I_{CEs} to filter out pipe defects because the currents created by emitter-collector shortening cannot be distorted by base-collector leakage. Although, increasing the Si cap layer thickness helped to reduce the generation of pipe defects this is not a suitable solution to the problem because f_T suffers substantially from this measure (Fig. 7). We performed a further experiment to enhance the mechanical stability of the transistors. By decreasing the

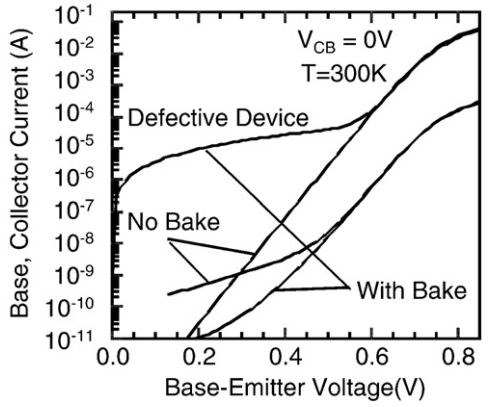

Fig. 6. Gummel plots of 4k arrays (A_E=4096×(0.21×0.84) μm^2) at V_{CB}=0 V for emitter depositions on the single wafer tool with/without pre-bake. The defective array shows a typical pipe behavior. Better base-current ideality for the array with bake results from a decreased tunneling component due to a reduced As indiffusion.

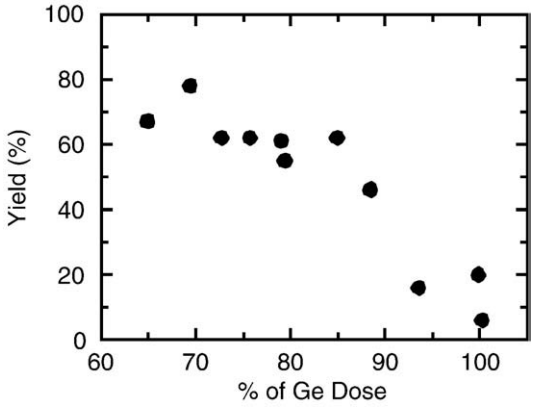

Fig. 8. Yield data of 12k HBT arrays vs. relative amount of Ge dose. The 100% Ge dose is equivalent to a 27.5 nm $Si_{0.8}Ge_{0.2}$ layer. Each symbol represents the yield value of one wafer. Emitter area of the array: A_E=12,800×(0.18×0.84) μm^2. Yield criterion: ideality of collector current nI_C (at V_{BE}=0.5 V)<1.1.

thickness of the Ge plateau we reduced the Ge dose of the SiGe:C base up to 35%. For this investigation, the reference Ge dose of 100% is equivalent to a 27.5 nm $Si_{0.8}Ge_{0.2}$ layer. As illustrated in Fig. 8, the array yield increases markedly when the Ge dose is lowered. Advantage can be taken from this improvement because the DC and RF device parameters are not changed essentially for the investigated SiGe thickness range.

In practice, a simple but effective way is required to fix this problem. Future investigations have to show whether this issue can be solved by changing a single process step, such as a new emitter deposition regime, or a complex of measures to eliminate the defect generation mechanism.

4. Summary

We demonstrated, that the way to fabricate the emitter layer of SiGe HBTs may have a significant impact on yield. Rapid thermal annealing of epitaxially-aligned highly-doped As emitters can generate crystal defects in the SiGe base. The formation of defects is enhanced when an interfacial oxide between emitter layer and base cap layer is avoided. In order to get high yield also with low residual oxide at the interface, we tested different changes of the process flow affecting the emitter deposition and the mechanical stability of the device. Additional investigations are necessary to find a generally acceptable, simple method to overcome this defect problem.

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