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A gm-boosted common-gate CMOS low-noise amplifier with high P1dB

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Abstract A 2.4-GHz transconductance (g_m)—boosted common gate (CG) low-noise amplifier (LNA) with a high 1-dB compression point (P1dB) is proposed. To overcome the constraint of conventional CG LNA for input-mismatching, RF filters consisting of band-stop and high-pass filter are used as a load and inter-stage matching components, respectively. Therefore, the g_m can be freely increased for a high gain and low noise figure (NF) without decreasing input impedance. Moreover, the linearity is also enhanced because band-stop filter load can reduce 2nd harmonics. The fully integrated LNA implemented by 0.18-μm RF CMOS technology delivers an input P1dB of −1 dBm, a power gain of 14.8 dB and a NF of 3.7 dB. The LNA consumes 8.2 mA at a supply voltage of 1.8 V.

Keywords Common-gate LNA · Low-noise amplifier · g_m boost LNA · High P1dB

1 Introduction

Orthogonal frequency-division multiplexing (OFDM) is a PHY-layer format suitable for future wireless communication systems due to its robustness against multi-path fading. Currently, OFDM has been used as the modulation scheme for numerous wireless communication standards near 2.4 GHz, such as wireless local area network (WLAN) and worldwide interoperability for microwave access (WiMAX) [1, 2].

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For a given bandwidth, modern OFDM systems select a large fast Fourier transform (FFT) size in order to have less susceptibility to multipath delay spread. The reduced subcarrier spacing due to the large FFT size, however, makes the system more vulnerable to flicker noise generated from RF components in direct conversion architecture.

It is because the noise degrades the signal-to-noise ratio (SNR) around the low frequency data subcarriers. Thus, from the LNA viewpoint, it should have a high gain and low noise figure for following a passive mixer which has better flicker noise performance.

The large FFT size also increases the peak-to-average power ratio (PAPR), which necessitates high linearity in the receiver when a gain-controllable LNA is not used. The input-referred 1-dB compression point (P1dB) could be an important figure-of-merit (FOM) of the LNA due to the existence of strong narrow-band interferences, such as IEEE 802.15.4 ZigBee signals in the 2.4 GHz band, as well as the increased PAPR [3]. However, the third-order intercept point (IP3) might not be an important FOM because adjacent and non-adjacent channel interferences are relatively low compared with other applications such as GSM and CDMA.

In order to achieve this, the common-gate (CG) LNA as shown in Fig. 1(a) is applicable because it features superior linearity and stability [4]. The CG amplifier can achieve high linearity due to current amplification [5], but the dependence of its gain and noise figure (NF) on its restricted transconductance (g_m) renders this topology unsuitable for the 2.4 GHz applications. Its input impedance is simplified as

$$Z_{IN} \cong \frac{1}{g_m} = 50\,\Omega \tag{1}$$

and when a backgate transconductance is negligible, the noise factor is [6]

$$F = 1 + \frac{\gamma}{\alpha R_S g_m} \quad (2)$$

where γ is coefficient of the channel thermal noise, R_S is input impedance and α is defined as the ratio of the gm and the zero-bias drain conductance, g_{d0}. In order to achieve a high gain and low NF, g_m should be increased, which degrades the 50 Ω input-impedance matching for the conventional CG LNA.

Typically, CG LNAs that have increased g_m are a capacitor cross-coupled configuration and transformer-coupled g_m-boosted topology as shown in Fig. 1(c) and (d) [7–9]. Both architectures utilize inverting gain of $-A$, as conceptually shown in Fig. 1(b), which is inserted between gate and source terminals. It boosts g_m to $(1 + A)$ g_m. However, capacitor cross-coupled topology consumes large bias current because it can only be applicable to differential structures. In addition, A is less than one because of the capacitor divider between C_{gs} and coupling capacitor, C_C [9].

The transformer-coupled g_m-boosted topology also has a limitation of A, which is given as $kn = k\sqrt{L_S/L_P}$. A large value of n is not feasible due to the restrictions on the self-resonant frequency and non-idealities of the on-chip transformer [9].

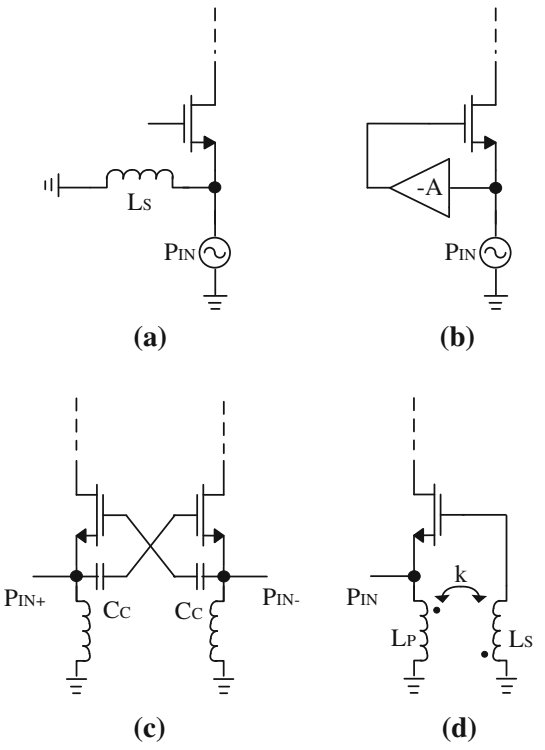

Fig. 1 Conventional LNA stages. **a** Conventional common-gate LNA, **b** gm-boosted common gate LNA topology, **c** capacitor cross-coupled LNA. **d** Transformer-coupled gm-boosted LNA

In this paper, we proposed a novel 2.4 GHz CMOS LNA that achieves freedom of boosting g_m. Moreover, the limitations of the common LNA topologies, namely low linearity, poor NF, and a gain-NF tradeoff are overcome in the proposed LNA by adopting a structure composed of a CG amplifier and a common-source (CS) amplifier with two filters.

2 Design of the proposed LNA

The schematic diagram of the proposed LNA is shown in Fig. 2. Two NMOS transistors, in a CG and CS configuration, are cascaded with two filters placed in between.

The CG configuration itself has wide bandwidth input matching and gain characteristics, which can seriously suffer from interferences coming from other wireless applications. These interferences may generate in-band harmonics in the following stages of the cascaded receiver chain. A band-stop filter (BSF) and a high-pass filter (HPF) are used between the two transistors. These filters not only provide a deep rejection ratio to minimize undesired frequency interferences, but also play an important role in increasing g_m without affecting input impedance. The BSF resonates at around 4 GHz and cutoff frequency of the HPF is about 1 GHz. The L_{S1} is used to provide a DC current path as well as to tune out the input capacitance at the required frequency. To obtain a good impedance match, L_{S1} and C_{gs1} should be selected such that they resonate at the center of the frequency band, 2.4 GHz.

Both the input and output have been matched to 50 Ω. The input impedance of the proposed LNA is given as

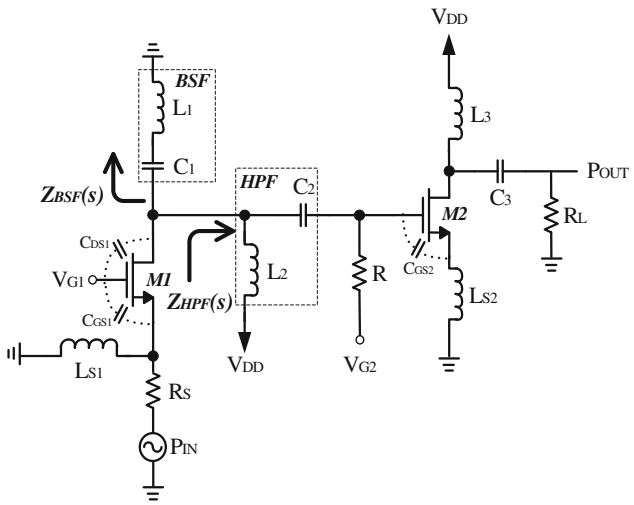

Fig. 2 Schematic diagram of the proposed LNA

$$Z_{IN} = \frac{1}{sC_{gs1}} // sL_{S1} // \frac{r_{ds1} + \left(Z_{BSF}(s) // Z_{HPF}(s) // 1/sC_{gd1}\right)}{1 + g_{m1} r_{ds1}} \quad (3)$$

$$= \frac{1}{sC_{gs1}} // sL_{S1} // \frac{1}{g_{m1}} // \frac{r_{ds1} + \left(Z_{BSF}(s) // Z_{HPF}(s) // 1/sC_{gd1}\right)}{1 - g_{m1}\left(Z_{BSF}(s) // Z_{HPF}(s) // 1/sC_{gd1}\right)}$$

$$= \frac{sL_{S1}}{1 + sL_{S1}\left(g_{m1} + sC_{gs1}\right)} // \frac{r_{ds1} + \left(Z_{BSF}(s) // Z_{HPF}(s) // 1/sC_{gd1}\right)}{1 - g_{m1}\left(Z_{BSF}(s) // Z_{HPF}(s) // 1/sC_{gd1}\right)} \quad (4)$$

where

$$Z_{BSF}(s) = sL_1 + \frac{1}{sC_1} \quad (5)$$

$$Z_{HPF}(s) = sL_2 // \left[\frac{1}{sC_2} + R // \left[\left(\frac{1}{sC_{gs2}} + sL_{S2}\right) + \frac{g_{m2}}{C_{gs2}} L_{S2}\right]\right] \quad (6)$$

When g_m is much larger than sC_{gs1} at the frequency of interest, the left term of (4) tends to $1/g_m$. If the overlap capacitance sC_{gs1} has been neglected in the interest of simplicity, the input impedance (4) is given as

$$Z_{IN} = \frac{1}{g_{m1}} // \frac{r_{ds1} + (Z_{BSF}(s) // Z_{HPF}(s))}{1 - g_{m1}(Z_{BSF}(s) // Z_{HPF}(s))} \quad (7)$$

As L_{S2} and C_{gs2} resonate far from the desired frequency and R is relatively large for DC biasing, the $Z_{HPF}(s)$ in the (6) can be approximated as sL_2. In this case, a parallel connection between $Z_{BSF}(s)$ and $Z_{HPF}(s)$ can, thus, be regarded as a purely reactive term.

$$Z_{BSF}(j\omega) // Z_{HPF}(j\omega) = \frac{j\omega L_2(1 - \omega^2 L_1 C_1)}{1 - \omega^2 C_1(L_1 + L_2)} = jX_S \quad (8)$$

By choosing a proper inductance of L_2, which makes the denominator of (8) as nearly zero and the numerator as a finite value, we can obtain a large purely reactive output impedance of the first stage through the BSF and HPF combination. The input impedance (4) can be rewritten using (8), and we get

$$Z_{in} = \frac{1}{g_{m1}} // \frac{r_{ds1} + jX_S}{1 - jg_{m1}X_S} = \frac{1}{\left(g_{m1} + \frac{r_{ds1} - g_{m1}X_S^2}{r_{ds1}^2 + X_S^2}\right) - j\left(\frac{1 + g_{m1}r_{ds1}}{r_{ds1}^2 + X_S^2} X_S\right)} \quad (9)$$

The imaginary portion of (9) can be neglected since $r_{ds1}^2 + X_S^2$ is much larger than $g_{m1} r_{ds1} X_S$. For the real portion, we can suppose that $r_{ds1} \ll g_{m1} X_S^2$, since the inductance of L_2 results in a value of X_S greater than r_{ds1}. This can be assumed due to the relative low output resistance of the short-channel MOS transistor which is generally around 500 Ω for a 0.18-μm CMOS process [10]. Thus,

$$Z_{in} \approx \frac{1}{g_{m1}\left(1 - \frac{X_S^2}{r_{ds1}^2 + X_S^2}\right)} \quad (10)$$

By using (10), the proposed LNA can be designed for high value of g_{m1}, maintaining input-impedance of 50 Ω using high X_S. Thus, it boosts the LNA gain without affecting the input-matching, in contrast to conventional CG LNA topology. The g_{m1} of the proposed configuration is designed to be 60 mS, while the conventional topology restricts its value to 20 mS for 50 Ω input impedance-matching as shown in (1).

Based on the assumption that the second stage noise can be neglected due to the high gain of the first stage, the noise factor can be represented by (2). While the NF of a conventional CG LNA is high due to restricted g_m of 20 mS, the design approach used in this topology provides a way to control the value of g_m for lowering the noise factor.

The proposed design also provides relatively high linearity over the required bandwidth by using current amplification in the first stage, which can eliminate V–I converters in a CS amplifier that often result in non-linearity. Moreover, The BSF resonated at around 4 GHz highly reduces second harmonics of the signal which degrade the linearity.

3 Experimental results

The circuit was fabricated using 0.18-μm CMOS technology. The following measurements were made using on-wafer

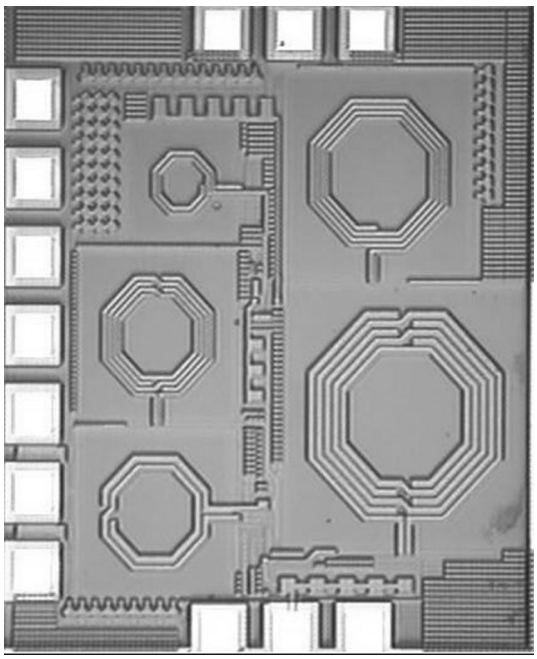

Fig. 3 Photograph of the fabricated device

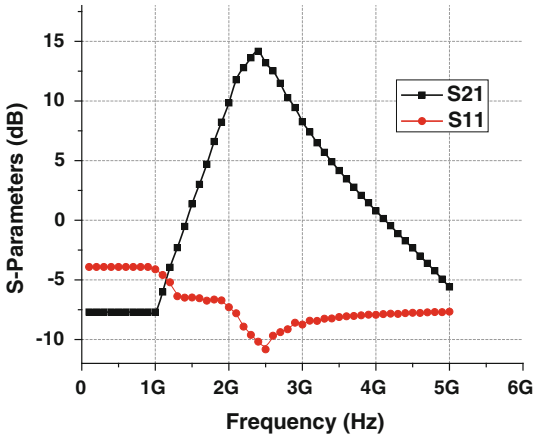

Fig. 4 Measured power gain and reverse isolation

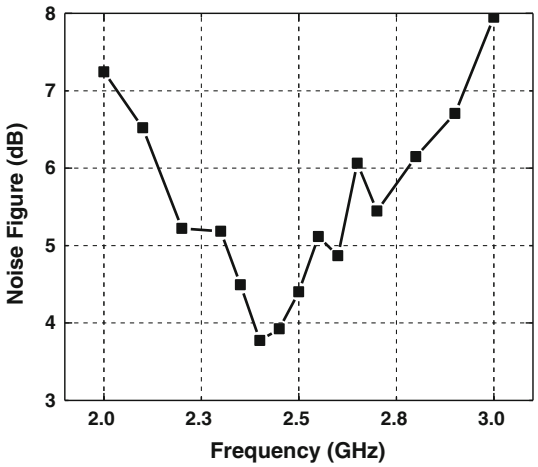

Fig. 5 Measured noise performance

probing. The photograph of the fabricated LNA with all on-chip components is shown in Fig. 3. The chip dimensions of the LNA are 1.07 × 1.2 mm^2 including the probe pads. It is biased on 8.2 mA from a 1.8-V supply voltage.

S-parameters, as shown in Fig. 4, were measured to characterize the LNA. The design achieved a power gain of 14.8 dB. Both input and output reflection coefficients are −8.3 and −11.1 dB, respectively. The frequency offset of reflection coefficients is likely due to inaccurate modeling of inductor with path lines. The reverse isolation of about −36 dB is achieved at 2.4 GHz. The reverse isolation is good due to 2nd stage amplifier.

Figure 5 shows the measured NF performance for the proposed LNA. A minimum noise figure of 3.7 dB was achieved. The input-referred P1dB point of −1 dBm was measured over the operating frequency range as shown in Fig. 6.

The fabricated LNA shows a very high input P1dB with high gain and relatively low power consumption. The NF is

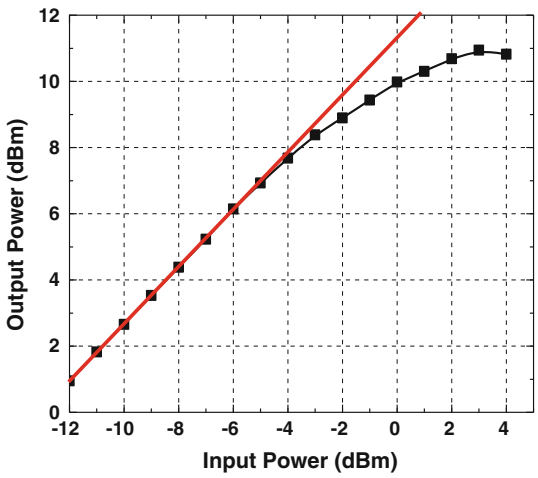

Fig. 6 Measured P1dB

slightly high because fully integrated on-chip inductors used in the proposed LNA have low quality factors.

4 Conclusion

A high input P1 dB of -1 dBm achieved by combining CG amplifier and CS amplifier is demonstrated. This design breaks the restriction of low transconductance for input-matching of a conventional CG LNA by using BSF and HPF between two amplifiers. This feature makes it possible to obtain a high gain and low NF simultaneously through relatively high g_m. The measured NF performance of the LNA can be further optimized by using a low resistive layout technique for the inductors.

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