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A non-blocking wavelength routing ONoC based on two-dimension bus architecture

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ABSTRACT

With the improvement of silicon-based optical devices and on-chip optical technologies, optical network-on-chip (ONoC) is becoming a significant interconnection solution for its high bandwidth, low network latency and efficient energy utilization. Some bus-based ONoCs face the problems of high bus congestion, low network utilization, which leads to high network latency and an extra overhead in power dissipation. In this paper, a non-blocking wavelength routing ONoC based on two-dimension bus architecture (2DWR-bus) is proposed to solve the problem face by previous bus-based ONoCs, realize multiple IP cores communicating with the same destination IP core simultaneously. The network simulation is carried out for the 16 cores and 64 cores ONoC under synthetic traffics. The end-to-end (ETE) delay and saturation throughput performance are evaluated and compared between 2DWR-bus and similarly-configured ONoCs. Netrace is used in the simulation to evaluate the network performance under realistic scientific application benchmarks. The insertion loss and required laser power for 2DWR-bus is calculated and made a comparison. The evaluation result shows that 2DWR-bus ONoC has better network performance when compared with other equivalent ONoCs, especially under high network offered load.

1. Introduction

Optical network-on-chip (ONoC) is a promising interconnection solution to solve the problem faced by electronic network-on-chip (ENoC) [1] for its high bandwidth and low energy consumption. In recent years, many high-performance yet energy-efficient ONoCs has been proposed, such as Firefly [2], Corona [3], ATAC [4], PHENIC [5] and Chameleon [6] etc. Photonics can achieve bandwidth density orders of magnitude higher than electronics with the use of various optical multiplexing technologies, such as wavelength-division multiplexing (WDM) [7], time-division multiplexing (TDM) [8] etc.

Single-write-multi-read (SWMR) [4,9] and Multi-write-single-read (MWSR) [3] are two frequently-used bus structures in several bus-based ONoC designs. SWMR avoids the need for global arbitration by preventing write contention. MWSR is good at reusability in the design. However, SWMR-based ONoC suffers from high power consumption. MWSR-based ONoC suffers from high link congestion, which leads to bad network performance [10].

In this paper, a non-blocking wavelength routing ONoC based on two-dimension bus architecture (2DWR-bus) is proposed to solve the problems face by previous bus-based ONoCs. By employing the active wavelength routing in X-dimension and the passive wavelength routing in Y-dimension, 2DWR-bus ONoC realizes non-blocking communications for the entire network and supports multiple source IP cores communicate with a destination IP core simultaneously. The network performance of 2DWR-bus is evaluated and compared with the equivalent OCS-mesh, OCS-torus and OCS-ring ONoCs under several synthetic traffics and realistic scientific application benchmarks of netrace. The maximum insertion loss and laser power for 2DWR-bus under 16 cores and 64 cores are also calculated respectively. 2DWR-bus achieves admirable insertion loss and laser power requirement performance compared with the OCS-mesh and OCS-torus ONoC under all conditions.

The rest of the paper is organized as follows. Section 2 introduces the related work. Section 3 presents the network architecture design and wavelength assignment for 2DWR-bus. Section 4 introduces the communication process between cores and gives the communication flow diagram. Section 5 evaluates and analyzes the network performance of 2DWR-bus. Conclusions and acknowledgments are given in the rest section.

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2. Related work

With the rapid development of high performance computing (HPC), Network-on-Chip (NoC) architectures [11,12] have been proposed as a promising solution to meet the performance and design productivity requirements of these complex HPC systems. Compared with System-on-Chip (SoC), NoC has the advantage of better network communication performance, reconfigurability, scalability and higher parallel processing capability. In the last few years, many research groups [13,14] including our group [15,16], researched the design and innovation of NoCs including various types of network architectures, topologies, router designs, routing algorithms, flow-controls and thermal model etc.

Future high-performance chips are expected to combine more and more components each integrated together to satisfy larger and more complex applications' power and performance requirements. Thus, to achieve significant and scalable solution to the interconnect delay problem, real fundamental changes in system interconnect, and fabrication technologies are needed. As predicted by the ITRS roadmap [17], the NoC component is gradually becoming the bottleneck of HPC performance, with several limiting factors, such as power consumption, crosstalk, latency, area, bandwidth, scalability etc.

To eliminate the problem faced by NoC, may researcher focus on the novel interconnect technologies. One of the solutions is adopting optical interconnect. It can provide higher bandwidth and lower latency with distance–independent power consumption [18,19]. In recent years, with a growing interest in addressing the issues of photonic and CMOS devices integration [20,21], and developing in new applications for a converged electronic-photonics IC platform [22–26], optical interconnect technology is significantly improved.

Optical Network-on-Chip (ONoC) is a novel concept enabling high bandwidth especially when combined with WDM [7] to concurrently transfer multiple parallel optical stream of data through a single waveguide, which contrast with ENoC that requires a unique metal wire per bot stream. ONoC offers a potentially disruptive technology solution with fundamentally low power dissipation that remains independent of capacity while providing more bandwidth at near speed-of-light transmission latency. Furthermore, with wavelength routing and various multiplexing technology, such as WDM, TDM [8], and mode division multiplexing (MDM) [27], ONoC has huge design and improvement potential. More and more high performance yet energy efficiency ONoC architectures will come out and be practical utilized in the near future.

Until now, many ONoCs with character of low power consumption, high bandwidth, resistance to electromagnetic interference and reduced signal crosstalk have been proposed. Yan Pan et al. present a hierarchical network topology called Firefly. Firefly consists of clusters of nodes that are connected using conventional, electrical signaling while the inter-cluster communication is done using nanophotonics-exploiting the benefits of electrical signaling for short, local communication while nanophotonics is used only for global communication to realize an efficient on chip network. The inter-cluster crossbar is realized by single-write-multi-read shared waveguide [17]. Vantrease et al. also propose an architecture named Corona which uses multi-write-single-read to perform crossbar, due to the existence of contention, optical token arbitration scheme is used [18]. The abovementioned ONoC are both bus-based, so they have to take corresponding measures to deal with contention and high power consumption problems.

Various designs of ONoC use optical circuit-switching (OCS) [28]. Fig. 1 shows the communication process of OCS-based ONoC. Many previous OCS-based ONoC employ the mesh topology for its simplicity and predictable scalability in terms of performance and power consumption. However, OCS-based mesh ONoC suffers from long latency and low throughput due to the high contention probability. Once the path from the source node to the destination node is reserved by a setup packet, this path will be exclusively occupied by this pair of communication nodes. As a result, other setup packets requiring any part of this path will be blocked, which leads to a high contention probability. For OCS-based ONoC, the high bandwidth utilization can only be achieved when the data is large, since it always needs to establish a path before the transmission and the use of path is unshared.

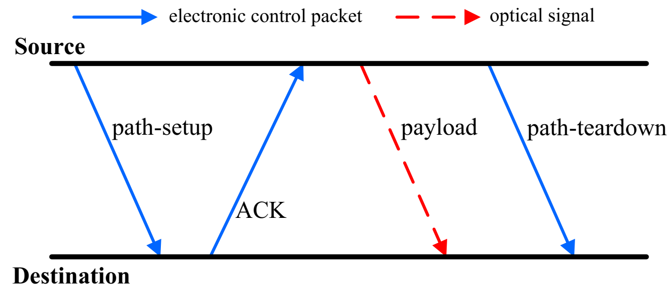

Fig. 1. Communication process of OCS-based ONoC.

3. Network architecture and wavelength assignment

2DWR-bus consists of three parts: node architectures, X-dimension bus architecture and Y-dimension bus architecture, as Fig. 2 shows. A node architecture includes four parts: an intellectual property (IP) core, an electronic crossbar, an E/O O/E unit and local buffers. All IP cores are placed in electrical layer uniformly. The electronic crossbar is employed to exchange the packet between IP core, local buffers and E/O O/E unit. E/O receiver unit consists of several photonic detectors and O/E transmitter unit consists of several photonic modulators, they are used to make optical-to-electric signal conversion. In one node architecture, there are m local buffers. Local buffers are employed to store the packets which have the requirements of Y-dimension communication. Some of these packets are transmitted to the node as an intermediate one in X-dimension communications, the others are generated from the local node and will be transmitted to the destination node in Y-dimension. Packets from different source nodes will be reconfigured logically according to their destinations in the local buffers, then each of them will be modulated to different wavelength signals according to its destination and transmitted to the destination node simultaneously in Y-dimension communications.

An X-dimension bus includes several active microring resonators (MR) [18, 29, 30] and a waveguide, as shown in Fig. 2. X-dimension bus is employed to realize the X-dimension communication. Active MRs need a control packet to set it to the on-state before the optical signal transmitted to its destination node. Fig. 3 shows the parallel switching element and crossing switching element for active microring resonator. In one X-dimension bus, packets from different source nodes are modulated by different wavelengths. Thus, packets from different source nodes can be transmitted to a same destination node simultaneously. For example, in a 4×4 2DWR-bus's X-dimension communications, all packets generated from node 0, 1, 2 and 3 will be modulated by wavelength λ_0, λ_1 λ_2 and λ_3 respectively, the rest are deduced by analogy. Table 1 shows the wavelength assignment for X-dimension communication.

A Y-dimension bus includes several passive MRs, passive broadband MRs (BMR) [31–34] and a waveguide, as shown in Fig. 2. Y-dimension bus is employed to realize the Y-dimension

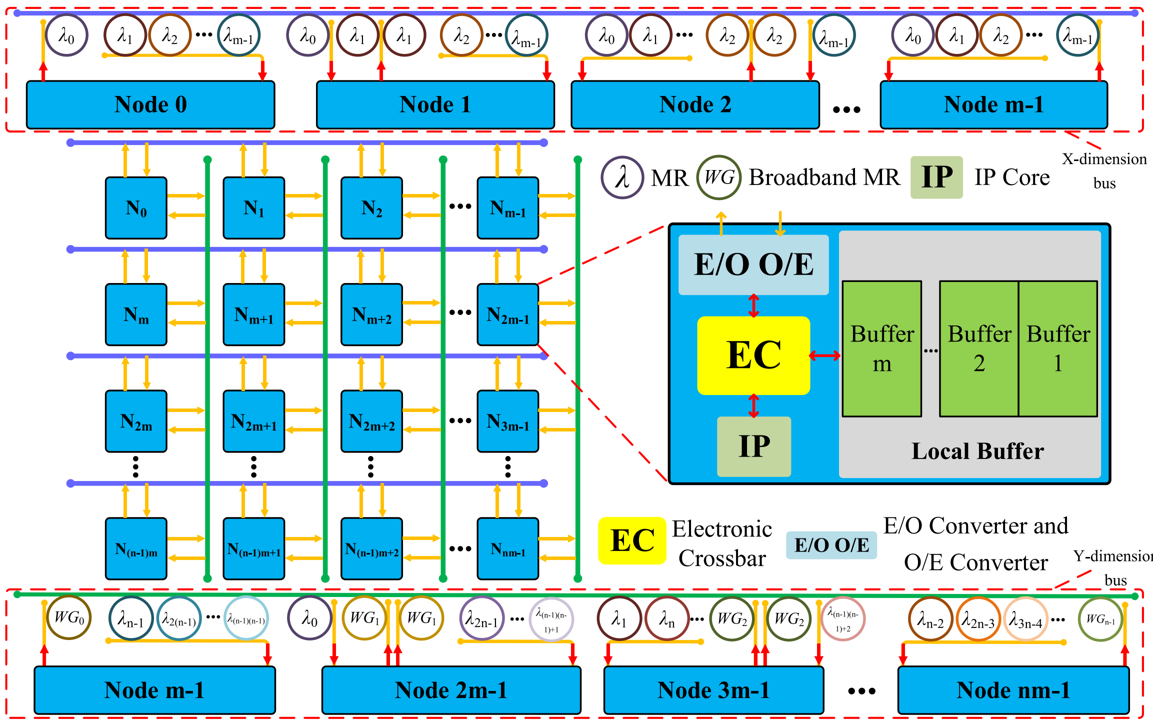

Fig. 2. Schematic of the m*n 2DWR-bus architecture.

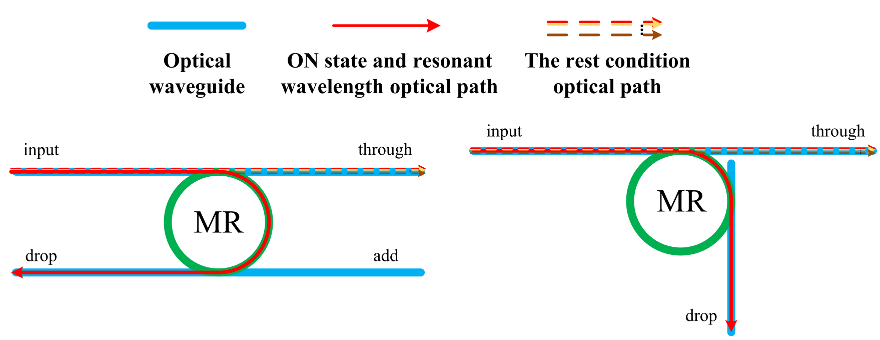

Fig. 3. Parallel switching element and crossing switching element for active MR.

Table 1
Wavelength assignment for *X*-dimension communication.

From	To: Node 0	Node 1	Node 2	…	Node m-1
Node 0	NULL	λ_0	λ_0	…	λ_0
Node 1	λ_1	NULL	λ_1	…	λ_1
Node 2	λ_2	λ_2	NULL	…	λ_2
…	…	…	…	…	…
Node m-1	λ_{m-1}	λ_{m-1}	λ_{m-1}	…	NULL

communication. Passive MRs are always in the on-state. When the optical data packets with the corresponding wavelength passing by the passive MRs, they will be coupled and transmitted to their destination node. Fig. 4 shows the parallel switching element and crossing switching element for the passive MR and BMR. BMR is used to transmit the optical data packets with different wavelengths at the same time. In one *Y*-dimension bus, packets with different destination nodes are modulated by different wavelengths. With a special wavelength assignment, packets from different source nodes can be transmitted to a same destination node simultaneously. Table 2 shows the wavelength assignment for *Y*-dimension communication.

4. Communication process

X–Y routing algorithm is used in the communication for its simple implementation and deadlock freedom. Assuming nodes are arranged from coordinate (0, 0) to $(m-1, n-1)$ in the network. There are three communication circumstances for 2DWR-bus ONoC:

- Only active *X*-dimension communication: The source node (X_s, Y_s) and the destination node (X_d, Y_d) are in the same *X*-dimension ($Y_s = Y_d$). Firstly, a control packet is sent to the destination node and inform the corresponding MR turn into the resonant state. Secondly, the packet is modulated by the wavelength according to the wavelength assignment table for *X*-dimension communication. Then the signal is injected into the *X*-dimension bus and transmitted to the destination node.
- Only passive *Y*-dimension communication: The source node (X_s, Y_s) and the destination node (X_d, Y_d) are in the same *Y*-dimension ($X_s = X_d$). The packet is modulated by the wavelength according to the wavelength assignment table for *Y*-dimension communication. Then the signal is injected into the *Y*-dimension bus and transmitted to the destination node.
- Combining *X–Y* dimension communication: The source node (

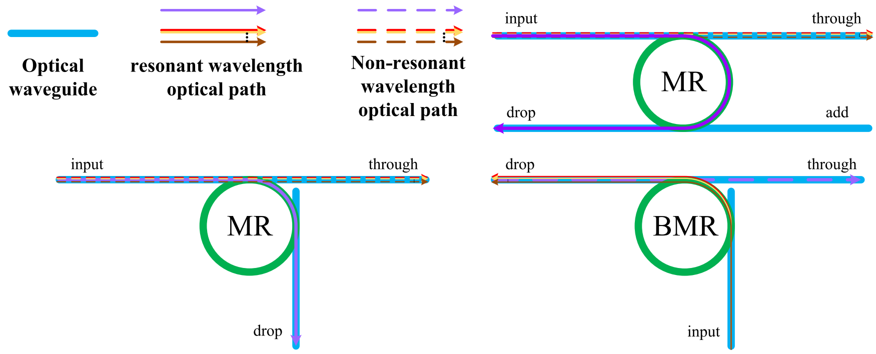

Fig. 4. Parallel switching element and crossing switching element for passive MR and BMR.

Table 2
Wavelength assignment for *Y*-dimension communication.

	To				
From	**Node m-1**	**Node 2m-1**	**Node 3m-1**	**…**	**Node nm-1**
Node m-1	NULL	λ_0	λ_1	…	$\lambda_{(n-1)-1}$
Node 2m-1	λ_{n-1}	*NULL*	λ_n	…	$\lambda_{2(n-1)-1}$
Node 3m-1	$\lambda_{2(n-1)}$	λ_{2n-1}	NULL	…	$\lambda_{3(n-1)-1}$
…	…	…	…	…	…
Node nm-1	$\lambda_{(n-1)(n-1)}$	$\lambda_{(n-1)(n-1)+1}$	$\lambda_{(n-1)(n-1)+2}$	…	NULL

Table 3
Simulation parameter configuration.

Parameter	**Value**
Clock Frequency(GHz)	1
Ack Packet Length(bit)	32
Path Setup Packet Length(bit)	32
Optical Packet Length(bit)	1024

X_s, Y_s) and the destination node (X_d, Y_d) are in the different *X*-dimension and *Y*-dimension ($X_s \neq X_d$, and $Y_s \neq Y_d$). Firstly, the packet is transmitted to the intermediate node (X_d, Y_s) with *X*-dimension communication. Secondly, the packet is stored into the local buffer queue according to its destination. Then the packet is transmitted to the destination node with *Y*-dimension communication.

Fig. 5 shows the flow diagram of 2DWR-bus's communication process.

5. Network performance evaluation

In this section, we present the results of the performance evaluation of the example 2DWR-bus in terms of end-to-end delay (ETE delay) and saturation throughput under the synthetic traffics, normalized execution speed and ETE delay under the realistic scientific traffic. We contrast 2DWR-bus with the similarly-configured OCS-mesh, OCS-torus and OCS-ring ONoCs. In addition, we also calculate the optical insertion loss and required laser power consumption for 2DWR-bus and make the comparisons.

In order to evaluate the performance improvement of 2DWR-bus, we build the example 2DWR-bus model with OPNET by modeling ONoC in system level, deploying its traffic model, topological structure, packet format, and other parameters. Table 3 shows the parameter configuration for 2DWR-bus and other ONoCs.

We compare the ETE delay and saturation throughput performance between 2DWR-bus, OCS-mesh, OCS-torus and OCS-ring under uniform and hotspot traffic patterns. Figs. 6–9 show the comparison results.

The simulation results show that under all conditions 2DWR-bus achieves better ETE delay and saturation throughput performance than OCS-mesh, OCS-torus and OCS ring ONoCs. When the scale of the network is small, OCS-torus ONoC has almost the same network performance compared with 2DWR-bus under uniform traffic; there is great gap of the network performance between

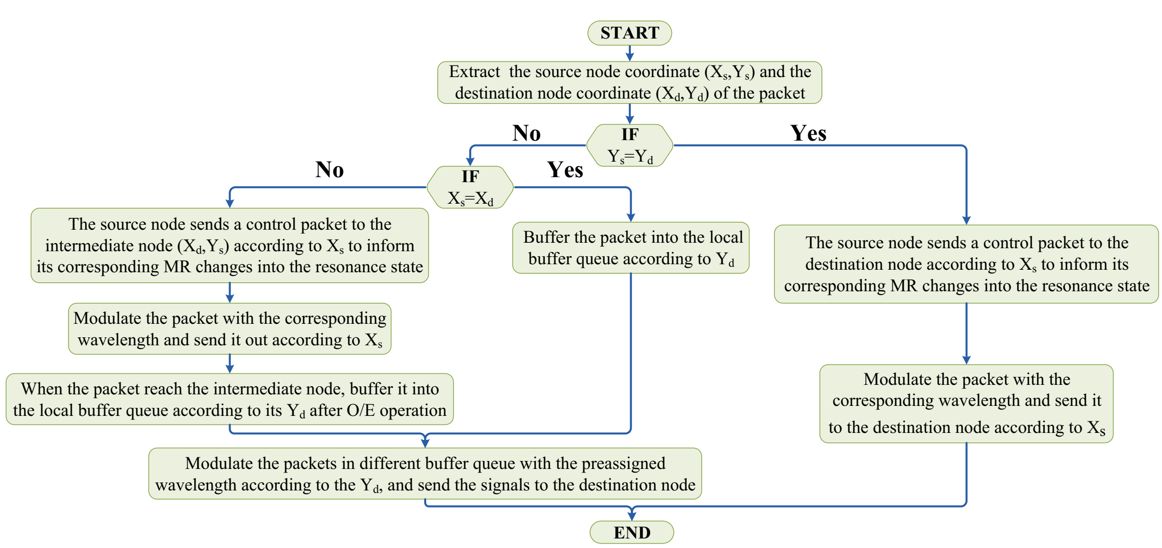

Fig. 5. Flow diagram of 2DWR-bus communication process.

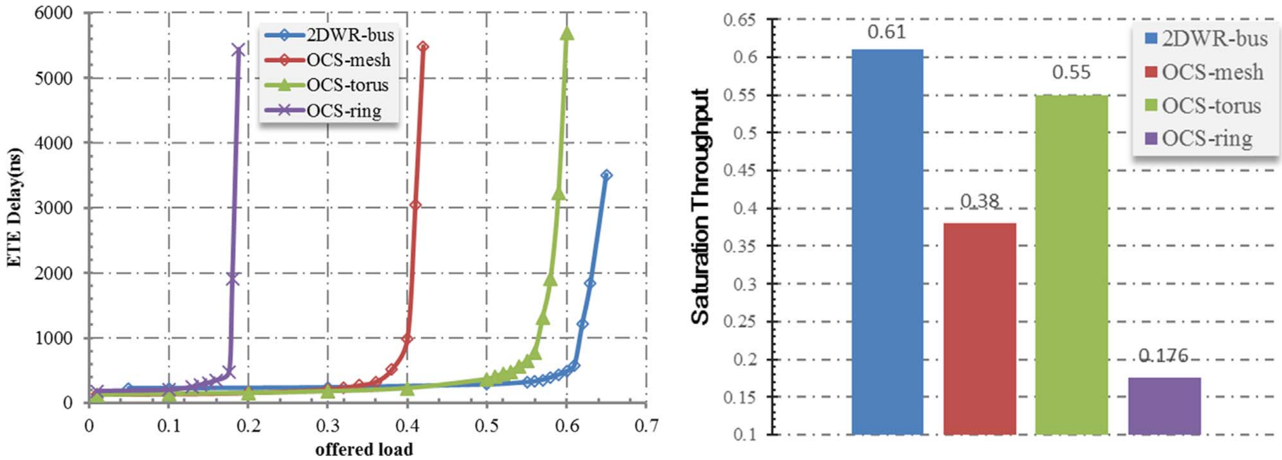

Fig. 6. ETE delay and saturation throughput comparison for 16 cores scale (4*4) under uniform traffic.

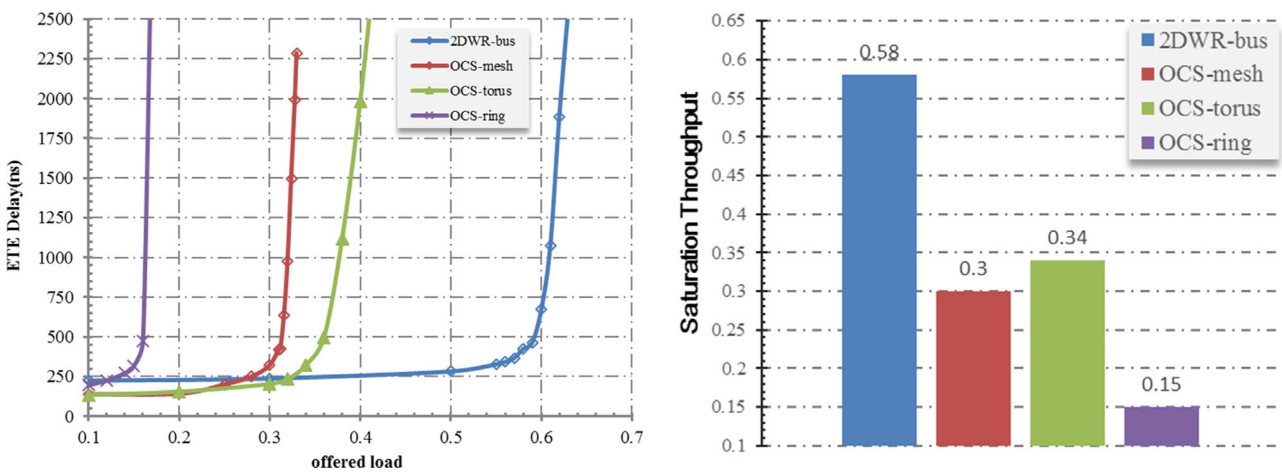

Fig. 7. ETE delay and saturation throughput comparison for 16 cores scale (4*4) under hotspot traffic.

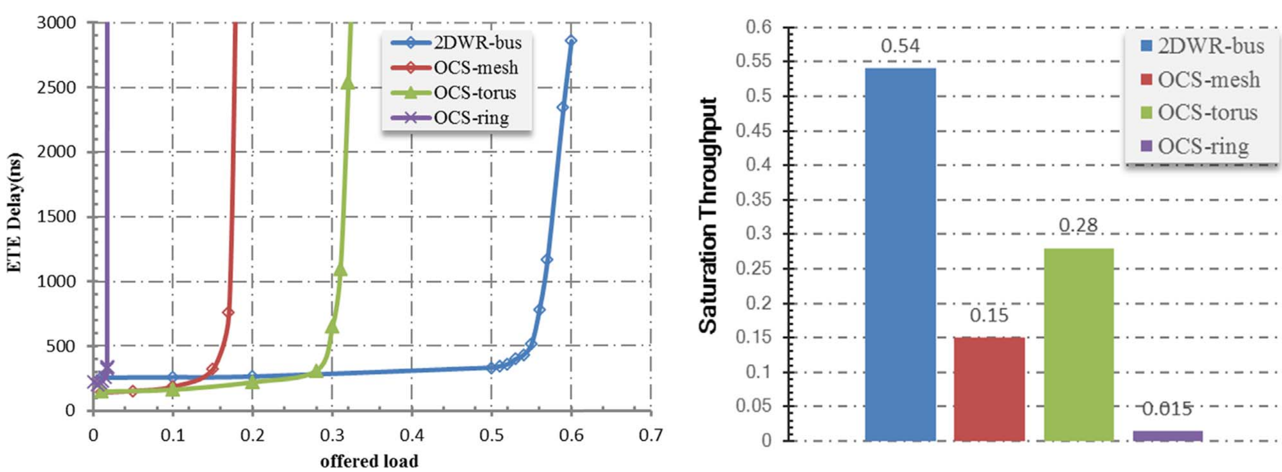

Fig. 8. ETE delay and saturation throughput comparison for 64 cores scale (8*8) under uniform traffic.

2DWR-bus and other ONoCs under hotspot traffic, since there are more network congestions, 2DWR-bus can solve the blocking problem with the two-dimension communication. With the increase of network scale, there will be more network congestions and blocking problems. 2DWR-bus has admirable network performance compared with the other ONoCs under all traffic patterns. It is worth nothing that, the ETE delay and saturation throughput performance of 2DWR-bus have not much difference from 16 cores scale to 64 cores scale. It benefits from the characteristic of non-blocking communication in 2DWR-bus.

To deeply research the network performance of the proposed ONoC, netrace [35] is used in network performance evaluation. Netrace is a trace-based NoC evaluation methodology that captures and enforces the dependencies between network messages from a full-system. Netrace more accurately tracks full-system network-level performance metrics. Netrace is usually utilized to evaluate a 64 cores system. Nine realistic scientific application benchmarks from the PARSEC benchmark suite [36], blackscholes,

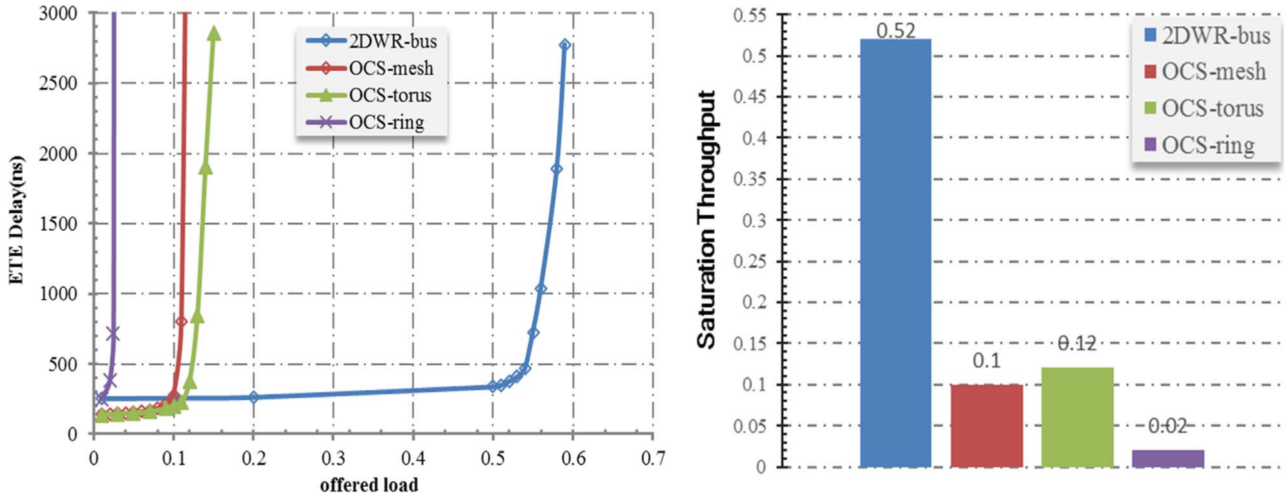

Fig. 9. ETE delay and saturation throughput comparison for 64 cores scale (8*8) under hotspot traffic.

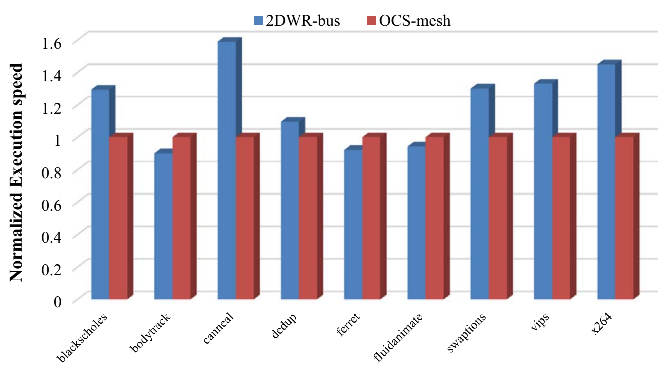

Fig. 10. Normalized execution speed comparison under various PARSEC benchmarks using netrace.

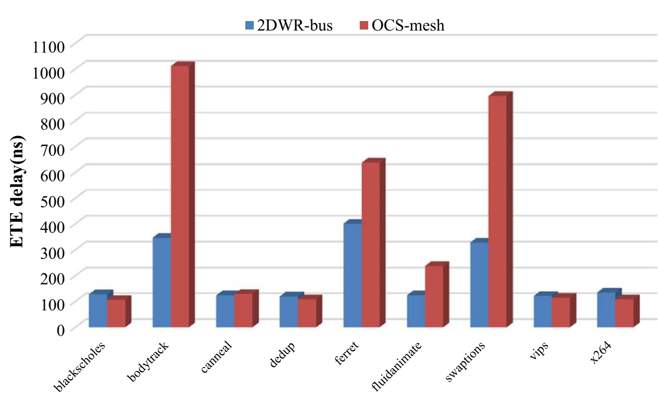

Fig. 11. ETE delay comparison under various PARSEC benchmarks using netrace.

bodytrack, canneal, dedup, ferret, fluidanimate, swaptions, vips and x264 are used, representing typical CMP applications with different sharing patterns, parallelization models etc.

The normalized execution speed is selected to evaluate and analysis the network performance of the 64-cores 2DWR-bus and the similarly-configured OCS-mesh ONoC. Different scientific benchmarks are running in the network simulation model. The execution time and ETE delay for different ONoC under different benchmarks are recorded. We set the execution time for OCS-mesh to 1, the execution time for 2DWR-bus is also normalized at the same time. The simulation result is shown in Fig. 10. In netrace, the offered load of each benchmark is quite low, such as the offered load of blackscholes can only be 9.09% [35]. Due to the low network offered load and the dependency tracking relationship, 2DWR has faster execution speed performance under bodytrack ferret and fluidanimate benchmarks.

The ETE delay is selected to further compare the network performance under netrace accurately. Fig. 11 shows the comparison result of ETE delay. 2DWRbus achieves better network ETE delay performance generally. 2DWR-bus reduces approximately 50% of the network ETE delay under bodaytrack, ferret, fluidanimate and swaptions benchmarks when compared with OCS-mesh ONoC, while OCS-mesh ONoC faces the problems of high network blocking and link congestions under higher network offered load.

Combing the simulation results of the normalized execution speed and ETE delay under all benchmarks using netrace, 2DWR-bus can achieve a better network work performance in the higher network offered load situations. The two-dimension wavelength routing strategy supports a non-blocking network communication and solves the serious blocking problem in OCS-mesh ONoC.

The optical insertion loss and optical energy consumption are other two important issues in ONoC designs. In the following, we calculate the optical insertion loss and the required laser power for 2DWR-bus ONoC and the equivalent OCS-mesh and OCS-torus ONoC. The OCS-ring ONoC is not included for there is no routing architecture in the ring topology, thus it has no optical insertion loss. Considering the worst case optical loss in the network, the optical power loss for a data transmission through a source-destination path is computed as follows [37]:

$$P_{Loss,Data}=P_{MR,DP}\times N_{on}+P_{MR,TP}\times N_{off}+P_B\times N_B+P_W\times L_l+P_{IL,WC}\times N_{WC}+P_{CR} \quad (1)$$

where N_{on} and N_{off} represent the number of resonators passed by the optical message, in the ON and OFF states respectively. N_B represents for the number of bending waveguide. L_l is longest optical link length, which is approximately 4.5mm in the 16 cores scale (4*4) ONoC and 9mm in the 64 cores scale (8*8) ONoC for each row and column. $N_{IL,WC}$ represents for the number of crossing waveguide in the ONoC design. The, hence the power required for a data transmission equals:

$$P_{Laser,Data}=N_W\times\frac{10^{(P_{RE\_min}+P_{Loss,Data})/10}}{P_{LE}\times P_{CW}} \quad (2)$$

N_w is the total number of wavelengths used in the ONoC, which can be 64 [38,39]. P_{RE_min} is the minimum power required by the receiver, which can be -22.3 dBm. P_{LE} is the laser efficiency, which can be 30%. P_{CW} is the coupling coefficient, which can be 90%. Other parameters, their implication and value are shown in Table 4.

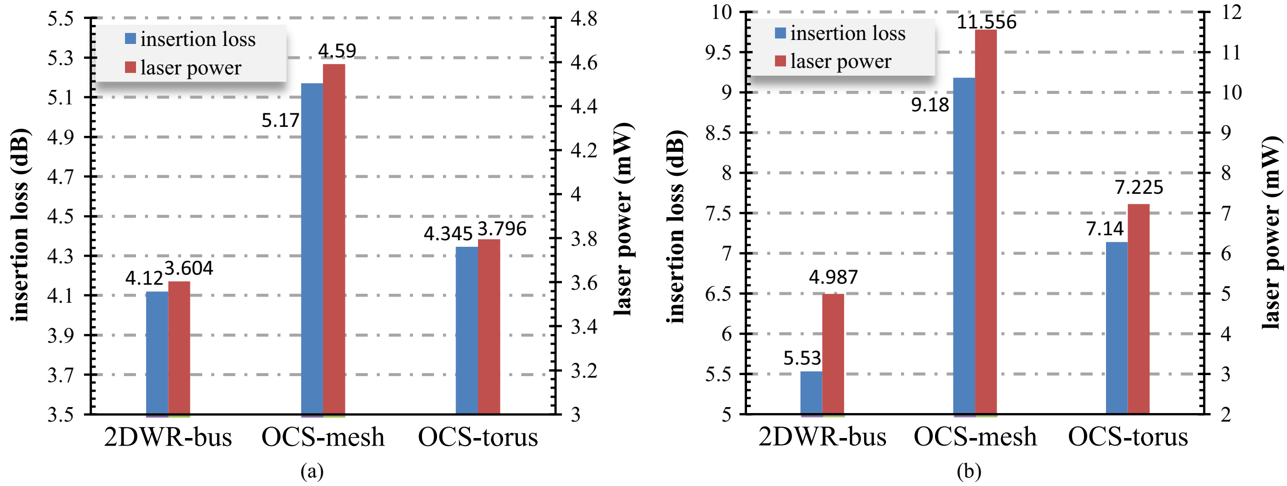

Fig. 12. Insertion loss and laser power comparison (a) 16 cores scale (4*4) (b) 64 cores scale (8*8).

Table 4
Parameters for optical power.

Parameter	Implication	Value
$P_{MR,DP}$	Drop-port insertion loss (MR)	0.5 dB [40–42]
	Drop-port insertion loss (BMR)	1.3 dB [31,43]
$P_{MR,TP}$	Through-port insertion loss	0.01 dB [2]
P_B	Waveguide bending loss	0.005 dB [44]
P_W	Waveguide propagation loss	0.5 dB/cm [45]
$P_{IL,WC}$	Waveguide crossing insertion loss	0.12 dB [44]
P_{CR}	Coupling loss	0.6 dB [9]

After calculation, the $P_{loss,Data}$ and $P_{laser,Data}$ for the 16-cores 2DWR-bus ONoC are approximately 4.12 dB and 3.604 mW, while the $P_{loss,Data}$ and $P_{laser,Data}$ for a equivalent OCS-mesh ONoC and OCS-torus ONoC are 5.17 dB, 4.59mW and 4.345 dB 3.796 mW respectively, as Fig. 12(a) shows. The $P_{loss,Data}$ and $P_{laser,Data}$ for the 64 cores 2DWR-bus ONoC are approximately 5.53 dB and 4.987 mW, while the $P_{loss,Data}$ and $P_{laser,Data}$ for a equivalent OCS-mesh ONoC and OCS-torus ONoC are 9.18 dB, 11.556 mW and 7.14 dB 7.225 mW respectively, as Fig. 12(b) shows. 2DWR-bus achieves admirable insertion loss and laser power requirement performance compared with the OCS-mesh and OCS-torus ONoC under all condidtions. Especially when the scale of network increasing from 16 cores to 64 cores. The insertion loss and required laser power of 2DWR-bus only increase 34.22% and 38.37%, while the insertion loss and required laser power of OCS-mesh and OCS-torus ONoCs increase 77.56%, 151.76% and 64.33%, 90.33% respectively.

6. Conclusion

In this paper, we propose a wavelength routing ONoC based on two-dimension bus architecture. 2DWR-bus ONoC employs active and passive wavelength routing in *X*-dimension and *Y*-dimension respectively. This ONoC realizes non-blocking communication, supports multiple source IP cores communicate with a destination IP core simultaneously. The proposed ONoC has batter network ETE delay and saturation throughput performance compared with the equivalent ONoCs under uniform and hotspot traffics in 16 cores and 64 cores conditions. In the netrace evaluation, 2DWR-bus achieves admirable normalized execution speed and ETE delay performance under several benchmarks which have the higher network offered load. 2DWR-bus also has a better optical insertion loss and optical power consumption performance in the comparison.

Our future work is to optimize the wavelength assignment and network structure to improve the 2DWR-bus to 3D (three-dimension) WR-bus and get a better network scalability.

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References

[1] O'Connor, Optical solutions for system-level interconnect, in: Proceedings of the 2004 International Workshop on System Level Interconnect Prediction, 2004, pp. 79–88.
[2] Y. Pan, P. Kumar, J. Kim, G. Memik, Y. Zhang, A. Choudhary, Firefly: illuminating future network-on-chip with nanophotonics, in: Proceedings of the 36th Annual International Symposium on Computer Architecture, 2009.
[3] D. Vantrease, R. Schreiber, M. Monchiero, et al., Corona: system implications of emerging nanophotonic technology, in: Proceedings of the International Symposium on Computer Architecture, 2008, pp.153–164.
[4] Kurian, George, et al., ATAC: a 1000-core cache-coherent processor with on-chip optical network, in: Proceedings of the 19th international conference on Parallel architectures and compilation techniques, ACM, 2010.
[5] Ben Ahmed, Achraf, Abderazek Ben Abdallah, PHENIC: silicon photonic 3d-network-on-chip architecture for high-performance heterogeneous many-core system-on-chip, Sciences and Techniques of Automatic Control and Computer Engineering (STA), 2013 14th International Conference on, IEEE, 2013.
[6] Le Beux, Sébastien, et al., Chameleon: channel efficient optical network-on-chip, Design, Automation and Test in Europe Conference and Exhibition (DATE), 2014, IEEE, 2014.
[7] Amitabha Banerjee, et al., Wavelength-division-multiplexed passive optical network (WDM-PON) technologies for broadband access: a review [invited], J. Opt. Netw. 4 (11) (2005) 737–758.
[8] G. Hendry, J. Chan, S. Kamil, L. Oliker, J. Shalf, L. Carloni, K. Bergman, Silicon nanophotonic network-on-chip using TDM arbitration, in: Proceedings of the 18th Annual IEEE Symposium High Performance Interconnects (HOTI), 2010, pp. 88–95.
[9] Kirman, Nevin, et al., Leveraging optical technology in future bus-based chip multiprocessors, in: Proceedings of the 39th Annual IEEE/ACM International Symposium on Microarchitecture, IEEE Computer Society, 2006.
[10] Le Beux, Sebastien, et al., A reconfigurable optical network on chip for streaming applications, Reconfigurable and Communication-Centric Systems-on-Chip (ReCoSoC), 2014 9th International Symposium on, IEEE, 2014.
[11] W.J. Dally, B. Towles, Route Packets, not Wires: On-Chip Interconnection Networks, DAC 2001, June 1822, Las Vegas, Nevada, USA, 2001.
[12] A. Ben Abdallah, M. Sowa, Basic network-on-chip interconnection for future gigascale MCSoCs applications: communication and computation orthogonalization, in: Proceedings of the Joint Symposium on Science, Society and Technology (JASSST2006), Dec. 4–9th, 2006, pp. 1–7.
[13] S. Parsricha, N. Dutt. Trends in emerging on-chip interconnect technologies, IPSJ Transaction on System LSI Design Methodology, vol. 1, August 2008, pp. 2–

17.
[14] Y. Hoskote, S. Vangal, A. Singh, N. Borkar, S. Borkar, A 5-GHz mesh interconnect for a teraops processor, vol. 27, Sept.–Oct. 2007, pp. 51–61.
[15] Na Zhang, Huaxi Gu, Yintang Yang, Dongrui Fan, QBNoC: QoS-aware bufferless NoC architecture, Microelectron. J. 45 (6) (2014) 751–758.
[16] Junhui Wang, Huaxi Gu, Yintang Yang, Kun Wang, Energy and buffer aware adaptive routing algorithm for network-on-chip, Microelectron. J. 44 (2) (2013) 137–144.
[17] SIA, International technology roadmap for semiconductors, Technical Report, 2003.
[18] D. Miller, Rationale and challenges for optical interconnects to electronic chips, Proc. IEEE 88 (6) (2000) 728–749.
[19] W. Bogaerts, P. Dumon, D.V. Thourhout, Low-loss, low-cross-talk crossings for silicon-on-insulator nanophotonic waveguides, Opt. Lett. 32 (19) (2007) 2801–2803.
[20] M. Beals, et al., White, process flow innovations for photonic device integration in CMOS, Proc. SPIE 6898 (689804) (2008) 689804–689814.
[21] S. Sahni, et. al., Silicon photonic integrated circuits, in: CLEO: Science and Innovations, OSA Technical Digest, Optical Society of America, 2012, (online).
[22] J.S. Orcutt, et al., Open foundry platform for highperformance electronicphotonic integration, Opt. Express 20 (11) (2012) 12222–12232.
[23] H.Ji, et al., Bulk silicon photonic wire for one-chip integrated optical interconnection, in: Proceedings of 2010 7th IEEE International Conference on the Group IV Photonics (GFP), 2010, pp. 96–98.
[24] K.Lee, et. al., 10 Gb/s silicon modulator based on bulksilicon platform for DRAM optical interface, in: The National Fiber Optic Engineers Conference, paper JThA033. C, 2011.
[25] A. Batten, et al., Building many-core processor-to-DRAM networks with monolithic CMOS silicon photonics, IEEE Micro 29 (4) (2009) 8–21.
[26] S. Jatar, et. al. Performance of parallel 4×25 Gbs transmitter and receiver fabricated on SOI platform, Presented at the Group IV Photonics (GFP), 2011 8th IEEE International Conference on, 2012, pp. 159–161.
[27] Lian-Wee Luo, et al., WDM-compatible mode-division multiplexing on a silicon chip, Nat. Commun. 5 (2014).
[28] Assaf Shacham, Keren Bergman, Luca P. Carloni, Photonic networks-on-chip for future generations of chip multiprocessors, Comput. IEEE Trans. 57 (9) (2008) 1246–1260.
[29] Z. Li, M. Mohamed, X. Chen, H. Zhou, A. Mickelson, L. Shang, M. Vachharajani, Iris: A hybrid nanophotonic network design for highperformance and low-power on-chip communication, J. Emerg. Technol. Comput. Syst. 7 (2) (2011) 8.
[30] H. Gu, K.Mo, J. Xu, W. Zhang, A low-power low-cost optical router for optical networks-on-chip in multiprocessor systems – on chip, in: Proceedings of the International Symposium VLSI, 2009, pp. 19–24.
[31] A. Biberman, B.G. Lee, N. Sherwood-Droz, M. Lipson, K. Bergman, Broadband operation of nanophotonic router for silicon photonic networks-on-chip, IEEE Photonics Technol. Lett. 22 (12) (2010) 926–928.
[32] Aleksandr Biberman, et al., Broadband silicon photonic electrooptic switch for photonic interconnection networks, Photonics Technol. Lett. IEEE 23 (8) (2011) 504–506.
[33] M. Bri'ere, B. Girodias, Y. Bouchebaba, G. Nicolescu, F. Gaffiot, I. O'Connor, System level assessment of an optical NoC in an MPSoC platform, in: Proceedings of the Design, Automation and Test Europe Conference and Exhibition, Apr. 16–20, 2007, pp. 1–6.
[34] X. Tan, M. Yang, L. Zhang, Y. Jiang, J. Yang, A generic optical router design for photonic network-on-chips, IEEE J. Light. Technol. 30 (3) (2012) 368–376.
[35] Joel Hestness, Stephen W. Keckler, Netrace: dependency-tracking traces for efficient network-on-chip experimentation, The University of Texas at Austin, Dept. of Computer Science, Tech. Rep, 2011.
[36] Bienia, Christian, et al., The PARSEC benchmark suite: characterization and architectural implications, Proceedings of the 17th International Conference on Parallel Architectures and Compilation Techniques, ACM, 2008.
[37] Koohi, Somayyeh, Shaahin Hessabi, All-optical wavelength-routed architecture for a power-efficient network on chip, 2012, 1-1.
[38] N. Kirman and J. Martínez, A power-efficient all-optical on-chip interconnect using wavelength-based oblivious routing, in: Proceedings of the 15th International Conference Architectural Support for Programming Langauge Operating System, 2010, pp. 15–28.
[39] K. Preston, N. Sherwood-Droz, J. Levy, et al., Performance guidelines for WDM interconnects based on silicon microring resonators, in: Proceedings of the Conference on Lasers and Electro-Optics (CLEO), May 2011.
[40] N. Biberman, X. Sherwood-Droz, K. Zhu, G. Preston, J. Hendry, J. Levy, H. Chan, M. Wang, Lipson, K. Bergman, Photonic network-on-chip architecture using 3D integration, Proc. SPIE 7942 (2011) 79420M–79421M.
[41] X. Zhang, A. Louri, A multilayer nanophotonic interconnection network for on-chip many-core communications, in: Proceedings 47th Design Automation Conference, Jun. 13–18, 2010, pp. 156–161.
[42] R. Dokania, A. Apsel, Analysis of challenges for on-chip optical interconnects, in: Proceedings of the 19th ACMGreat Lakes Symposium VLSI, 2009, pp. 275–280.
[43] Biberman, Aleksandr, et al., Silicon microring resonator-based broadband comb switch for wavelength-parallel message routing,LEOS 2007, 2007.
[44] Dana M. Vantrease, Optical tokens in many-core processors. Diss. University of Wisconsin–Madison, 2010.
[45] Michal Lipson, Guiding, modulating, and emitting light on silicon-challenges and opportunities, J. Light. Technol. (2005) 4222 23.12.