LOW LEAKAGE CNTFET FULL ADDERS

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***Abstract*— As the technology scales down to 32nm or below, the leakage power starts dominating the total power. Reduction of this leakage problem is the major problem, today's CMOS technology is facing. Hence researchers are looking for alternate technologies. The Carbon Nanotubes FET (CNTFET) is found to be a most promising device that becomes alternative or replacement for present CMOS technology. As the full adder is one of the major units of the ALU, it plays important role in speed and power consumption. In this paper several CNTFET full adder circuits are designed by applying different leakage power reduction techniques to reduce leakage power and to enhance the performance of the full adder circuit. Finally the full adder circuit with the proposed stacked single transistor leakage feedback technique was designed and proved that the proposed stacked single transistor leakage feedback CNTFET Full adder will reduce more leakage power with the same performance compared to all other techniques.**

Keywords—leakage power; full adder (FA); carbon nano tube FET (CNTFET); HSPICE.

I. INTRODUCTION

Technology scaling has resulted in a significant increase of leakage current in CMOS devices. In nano-scale CMOS devices, the major components of leakage current are sub-threshold leakage, gate direct tunneling leakage and reverse biased band-to-band tunneling junction leakage. The device design methods used to optimize a particular leakage component may increase another one. For example, in order to overcome the short channel effect due to scaling of channel length and supply voltage, the threshold voltage of the transistor is reduced to improve the drive current which also results in increase of sub-threshold leakage exponentially [1] hence designing a device to reduce total leakage in a circuit, while maintaining or improving circuit performance is becoming a challenging problem.

The CNTFET has been advocated as one of the possible alternatives to replace the conventional MOSFET due to its excellent performance characteristics. Moreover its operational principles and device structure are similar to those of a MOSFET device, thus showing excellent compatibility with CMOS manufacturing processes. In CNTFETs, ballistic or near-ballistic transport phenomena have been observed under low voltage, and the existing design infrastructure and fabrication process of CMOS-based MOSFETs can be also used for CNTFETs [2]. A CNTFET refers to a field-effect transistor that utilizes a single carbon nanotube or an array of carbon nanotubes as the channel material bridging the source and drain instead of bulk silicon in the traditional MOSFET structure.

The adder is one of the most critical components of a processor, as it is used in the Arithmetic Logic Unit (ALU), in the floating-point unit and for address generation in case of cache or memory access. The 1-bit full-adder cell is the building block of all these modules. Thus, designing low power and high performance full adder circuit is desirable. Several circuit techniques are proposed to reduce leakage power. This paper proposes new leakage power reduction technique to enhance the performance of the circuit.

II. THE CARBON NANO TUBE FET

A sheet made of carbon atoms arranged in a honeycomb lattice is called a graphene sheet. Carbon nanotube is formed by rolling the graphene sheet. Graphene is crystalline allotrope of carbon. In graphene, carbon atoms are densely packed in a regular sp^2-bonded atomic-scale chicken wire (hexagonal) pattern. This structure grants graphene its exciting electronic properties: over this two-dimensional carbon Nano world, electrons move almost freely at very high speeds, acting like mass less particles which means more efficient devices that will be able to be built a lot smaller than what silicon allows.

A CNT can act as a metal or a semiconductor depending on its chirality. A vector (m, n) connecting the centers of the two hexagons is called the chiral vector. If m=n or m-n=3i, where i is an integer, then CNT acts as metal otherwise it acts as a semiconductor [3].
The diameter of the CNT is given by [4]

$$D_{CNT} = \frac{\alpha\sqrt{3}}{\pi}\sqrt{n^2 + m^2 + mn} \qquad (1)$$

α =0.142 nm, the inter atomic distance between each carbon atom and its neighboring atom. (n, m) are the chirality of the CNT.

To design a circuit of best performance with an average power consumption and speed, the important parameter is the threshold voltage because this affects the switching speed, the current and leakage power. In CNTFET,

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by adjusting the diameter, the threshold voltage can be controlled and is given by [5]

$$V_{th} \approx \frac{E_g}{2q} = \frac{av_\pi}{\sqrt{3}qD_{CNT}} \quad (2)$$

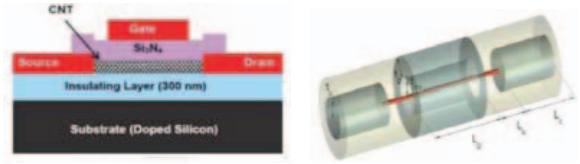
Where a = 2.49Å is the carbon to carbon atom distance

v_π is the carbon π-π bond energy in the tight bonding model

q =1.6 e-19 C is the electron charge

E_g is the energy gap

Hence by adjusting the diameter of CNT different transistors with different turn on voltage can be implemented.



(a) (b)

Fig.1 Geometry of CNTFET (a) planar (b) coaxial

There are several types of CNTFETS that have been fabricated. The geometry of the CNTFET may be planar and coaxial as shown in Fig. 1(a), 2(b).

III. Full Adder

Basically full adder is used in all arithmetic calculations. It is a key component of ALU where binary addition is the crucial part and ALU is the heart of Micro-Processor, DSP architecture and any data processing system. It plays main role in power consumption and speed because it involves carry propagation step throughout the operation. It takes three 1-bit numbers (A, B, C) as inputs and outputs two 1-bit numbers a sum and a carry. The basic full adder circuit with CNTFET is shown in the Fig.2. The CNTFET full adder (CNTFET FA) is designed by considering the chirality (10, 0) and the number of tubes is 3 for all the transistors.

IV. Low Leakage FA Designs

Lowering of supply and threshold voltage in modern portable devices however, leads to an increase in the leakage current [6]. The battery operated products like, mobile phones and laptop have long standby period, and therefore, reducing leakage current is necessary for long battery life because in the current technologies leakage power dominate over the dynamic power [7. To meet this challenge, many different circuit level techniques are designed to reduce the leakage power. All these circuit level leakage reduction techniques are applied to CNTFET-based Full Adder and these are presented in this section.

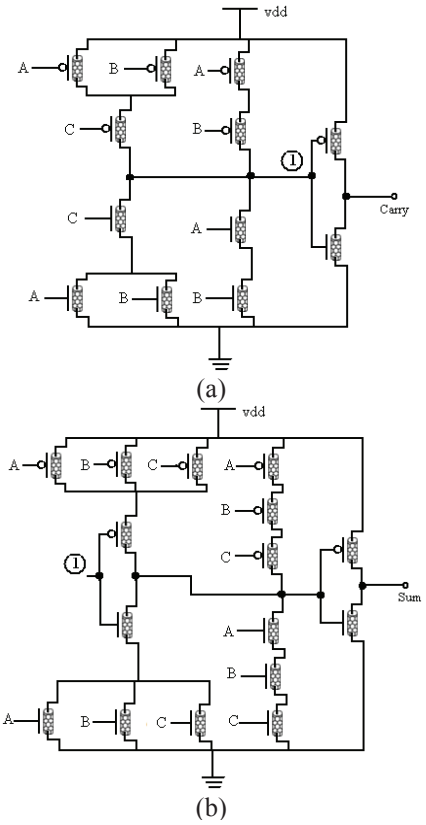


Fig.2 CNTFET FA (a) carry (b) sum

A. *Sleep CNTFET Full Adder*

In sleep technique high v_{th} cut-off transistors also called sleep transistors are added for pull-up or pull-down or for both networks from supply voltage or from ground [8]. High v_{th} transistors are used to reduce the delay. The CNTFET FA design using sleep techniques is shown in fig.3. During standby mode (sleep=logic high) transistors s1 and s2 are in OFF, cutting off the power, ground supplies. The circuit was designed by taking (5, 0) as chirality for s1, s2 transistors.

With this technique leakage power is minimized by a large amount but the main disadvantage of this technique is it will not retain the data during the standby mode.

B. *Leakage Feedback CNTFET Full Adder (LFB CNTFET FA)*

Leakage feedback (LFB) technique is used to maintain logic state during sleep mode [9]. The CNTFET FA design using Leakage feedback (LFB) technique, called LFB CNTFET FA is shown in fig.4. The M1, M2 are the sleep transistors and M3, M4 are the helper transistors which are used to maintain the logic during sleep mode. The transistors M3, M4 are driven by the output of an inverter the input of which is connected to the output of the circuit.

During the standby mode M1, M2 are OFF and one of the pull-up (M3) or pull-down (M4) parallel transistors turns ON.

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First case if the output is at 'logic high' , it will turns OFF M4 through the inverter, completely avoiding the leakage path from the ground power rail while M3 turns ON and maintaining the output logic by connecting to VDD power rail. In second case when the output is at 'logic low' it will turns ON the M4 transistor and turns OFF M3 transistor thereby avoiding the leakage path from VDD power rail and the output logic will be maintained. The LFB CNTFET FA circuit is designed by considering by considering (5, 0) as chirality and number of tubes are 2 for M1, M2, M3, M4 transistors. Drawback of this technique is too many transistors are added to retain the data during the sleep mode hence speed may be degraded.

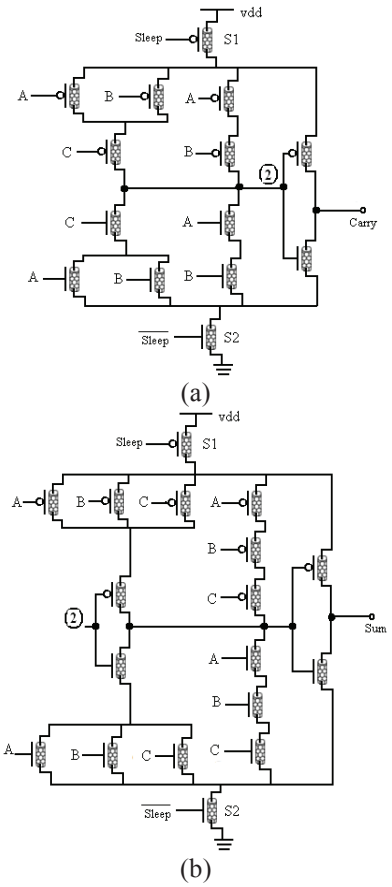

Fig.3 Sleep CNTFET FA (a) carry (b) sum

C. Leakage Feedback with Stack CNTFET Full Adder (LFBS CNTFET FA)

The Leakage feedback with stack (LFBS) [10] is a modified form of Leakage feedback technique. The CNTFET FA design using this LFBS technique is shown in Fig.5. This technique combines the advantage of the two techniques. Leakage feedback approach has a benefit of data retention and stacking is beneficial from the point of low power. Here stacking is used for the sleep transistors.

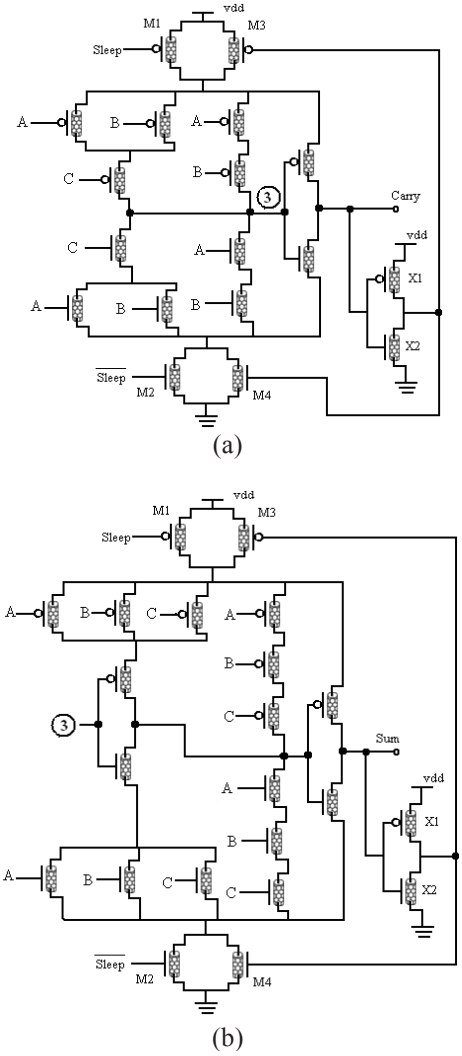

Fig. 4 LFB CNTFET FA (a) carry (b) sum

D. Sleepy Keeper CNTFET Full Adder (SK CNTFET FA)

In sleepy keeper (SK) technique [11] output is directly connected to M3 (NCNTFET) and M4 (PCNTFET) as shown in Fig.6. During the standby mode the sleep transistors M1 and M2 turn OFF. If the output is at 'logic high' then it will turns OFF M4 cutting off the ground rail and turns ON M3. If the output is at 'logic low', M3 will cut-off the VDD power rail and M4 turns ON to maintain the output logic. Hence with this technique leakage power is minimized by cutting of one of the power rails. This circuit is designed by considering (5, 0) as chirality for all M1, M2, M3, M4 transistors.

E. Single Transistor Leakage Feedback CNTFET Full Adder (ST LFB CNTFET FA)

In this single transistor leakage feedback (ST LFB) technique all n-type parallel transistors are used in pull-up and pull down paths as shown in Fig.7. Moreover a single p-type transistor is connected between lower n-type transistor and output [12]. During the sleep mode M1, M2 are in OFF.

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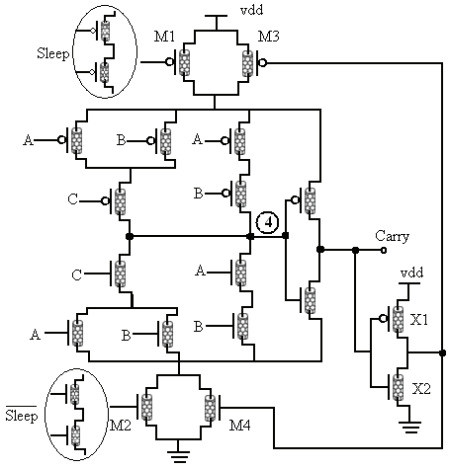
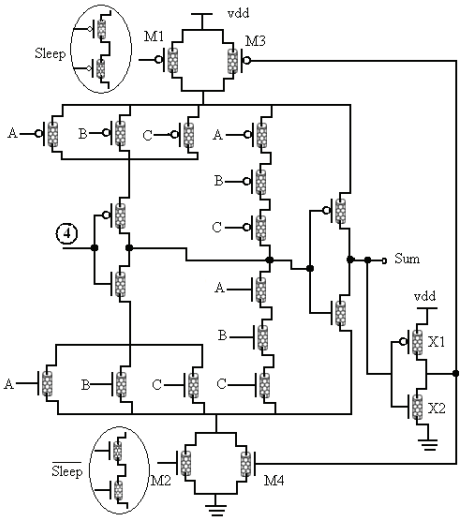
If the output is at 'logic high' then P1-OFF concurrently N2 is also turned OFF, thereby completely eliminating any leakage path from ground power rail while N1-ON and maintaining output logic by connecting to VDD power rail. In second case when output is at 'logic low' then P1-ON and will turn on N2 and this logic low turns OFF N1. In this way, pull up network is disconnected from VDD supply rail and pull down network is now connected to ground supply rail. By considering (5, 0) chirality for M1, M2, N1, N2 transistors and (2, 0) chirality for P1 transistor, full adder with single transistor leakage feedback technique is designed.



(a)

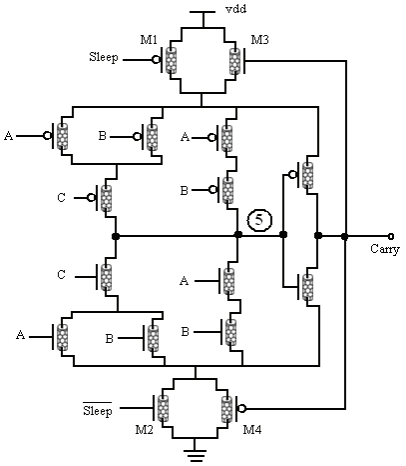


(b)

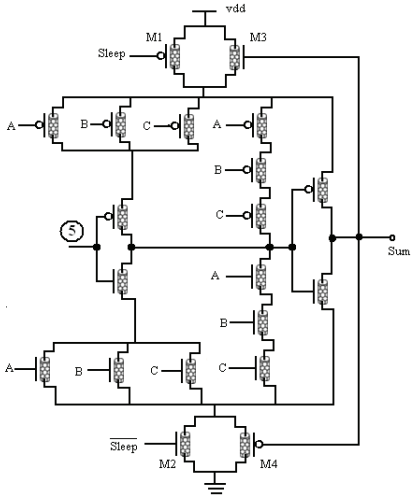
Fig. 5 LFBS CNTFET FA (a) carry (b) sum

F. Proposed Stacked Single Transistor Leakage Feedback CNTFET Full Adder (PSST LFB CNTFET FA)

Proposed stacked single transistor leakage feedback (PSST LFB) is the modified form of the single transistor leakage feedback technique. This technique is proposed by applying stacking effect for the single transistor leakage feedback technique as shown in Fig.8. The stacking is applied for the p-type transistor used to retain the data during the standby mode. The operation is same as that of single transistor leakage feedback technique. By using the stacked P-transistor (P1, P2) more leakage power is reduced as compared to the previous techniques. For stacked transistors P1, P2 number of tubes is one, chirality is (2, 0) is considered for design purpose.



(a)



(b)

Fig. 6 SK CNTFET FA (a) carry (b) sum

V. RESULTS

All the CNTFET full adder circuits explained above are designed and the simulations are done using Synopsys HSPICE tool at 32 nm technology with 0.9V supply. All the simulation results are tabulated as shown in the table1 and all the designs are compared in terms of leakage power, total power and delay as shown in fig.9, 10 and 11 respectively. From the table1 it is observed that 81.87% of the leakage power is reduced with the sleep CNTFET FA compared with

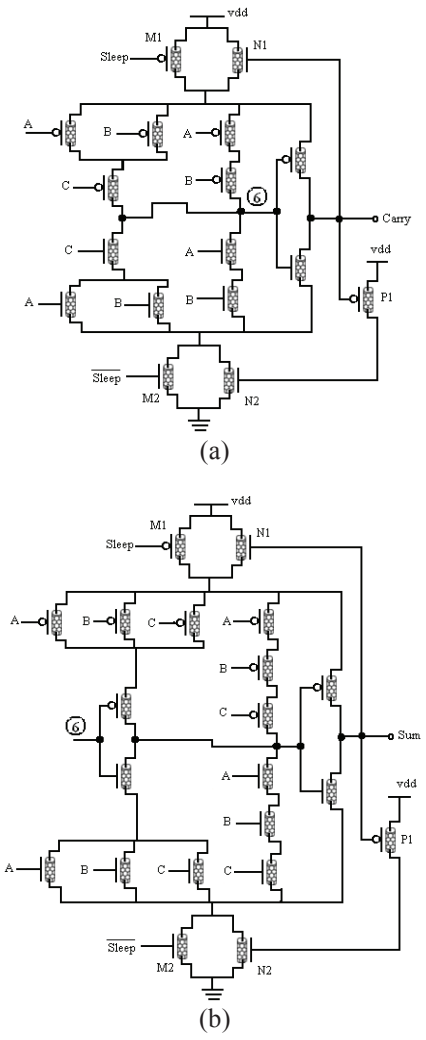


Fig. 7 ST LFB CNTFET FA (a) carry (b) sum

basic CNTFET FA, but the main disadvantage of this technique is that it is not going to retain the data during the standby mode. The LFB CNTFET FA reduces 52.29% of the leakage power, the LFB with Stack CNTFET FA reduces 54.84% of the leakage power, the SK CNTFET FA reduces 63.43% of the leakage power and the ST LFB CNTFET FA reduces 63.64% of the leakage power, compared with basic CNTFET FA. Finally the proposed Stacked-Single T Leakage Feedback (PSSTLFB) CNTFET FA reduces 65.83% of the leakage power compared with basic CNTFET FA, so this technique is better compared to all other techniques in terms of leakage power.

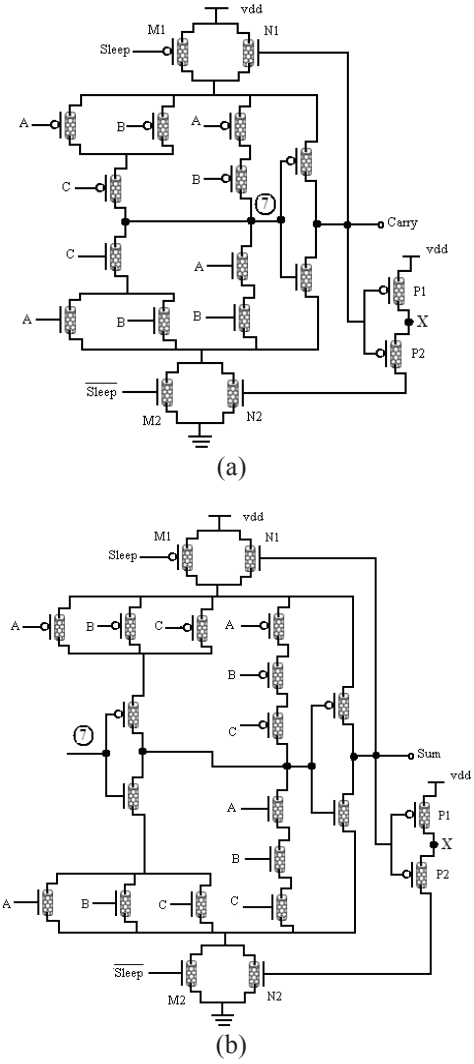


Fig.8 PSST LFB CNTFET FA (a) carry (b) sum

TABLE I. COMPARISON OF ALL THE DESIGNS

Sl.No	Design	Leakage power(nw)	Total Power(nw)	Delay (ns)
1	Basic CNTFET FA	0.192	0.192	65.414
2	Sleep CNTFET FA	0.0348	0.0372	62.271
3	LFB CNTFET FA	0.0916	0.0924	65.477
4	LFBS CNTFET FA	0.0867	0.0956	65.502
5	SK CNTFET FA	0.0702	0.0778	69.517
6	STLFB CNTFET FA	0.0698	0.0716	69.202
7 .	PSSTLFB CNTFET FA	0.0656	0.0762	69.402